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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,534	03/16/2000	Koji Suzuki		2400

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EXAMINER	
SEFER, AHMED N	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,534	SUZUKI, KOJI	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed September 21, 2005 has been entered; no new claims have been introduced.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. ("Yamazaki ") USPN 5,917,225 in view of Tanabe et al. ("Tanabe") US PG-Pub 2002/0072158.

Yamazaki discloses in figs. 6 and 9 a thin film transistor comprising semiconductor film or poly-silicon film (as in claim 12), a first gate insulating film 506/604 or silicon oxide film (as in claim 11), a second gate insulating film 507/603 and a gate electrode 509 formed on a surface of substrate, wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is made of a material or silicon nitride film (as in claim 11) for supplying hydrogen to said semiconductor film; said second gate insulating film being integrally formed over said first gate insulating film covering said semiconductor film; and said second gate insulating film covering said first gate insulating film in said regions not covered with said gate electrode, but does not specifically disclose an insulating film with a smaller film thickness in a region not covered with a gate electrode than one covered with a gate electrode.

Tanabe discloses (see fig. 3, par. 0077 and claim 1) a silicon nitride insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode.

Since Yamazaki and Tanabe are both from the same field of endeavor, Thin Film Transistors, Tanabe's teachings would have been recognized in Yamazaki's pertinent art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamazaki's device by incorporating Tanabe's teachings, since that would enlarge dielectric constant minimizing leakage as taught by Tanabe.

Regarding claim 16, Tanabe discloses a second insulating film having a smaller film thickness from an end position of said gate electrode covering said second insulating film.

4. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa ("Ogawa") JP 5-335578 (of record) in view of Tanabe.

Ogawa discloses in figs. 1-6 a thin film transistor comprising a semiconductor film or poly-silicon film (as in claim 12), a first gate insulating film 3 or silicon oxide film (as in claim 11), a second gate insulating film 4 and a gate electrode 5 formed on a surface of substrate 1, wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is made of a material or silicon nitride film (as in claim 11) for supplying hydrogen to said semiconductor film; and said second gate insulating film covering said first gate insulating film in said regions not covered with said gate electrode, but does not specifically disclose an insulating film with a smaller film thickness in a region not covered with a gate electrode than one covered with a gate electrode.

Tanabe discloses (see fig. 3, par. 0077 and claim 1) a silicon nitride insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode.

Since Ogawa and Tanabe are both from the same field of endeavor, Thin Film Transistors, Tanabe's teachings would have been recognized in Ogawa's pertinent art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Tanabe's teachings with Ogawa's device, since that would enlarge dielectric constant minimizing leakage as taught by Tanabe.

As for the said second gate insulating film being integrally formed over said first gate insulating film recited in claim 10, it carries no patentable weight In re Larson 144 USPQ 347 (CCPA 1965) (the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.)

5. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Tanabe.

Yamazaki discloses figs. 6 and 9 a thin film transistor comprising semiconductor film or poly-silicon film (as in claim 15), a first gate insulating film 506 or silicon oxide film (as in claim 14), a second gate insulating film 507 and a gate electrode 509 sequentially formed on one major surface of a substrate in that order, and an interlayer insulating film 518 having a thickness larger than that of said second gate insulating film in a region covered with said gate electrode,

said interlayer insulating film covering said gate electrode and covering said second gate insulating film in a region where said gate electrode is not formed, and wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is made of a material or silicon nitride film (as in claim 14) for supplying hydrogen to said semiconductor film; said second gate insulating film being integrally formed over said first gate insulating film covering said semiconductor film; and said second gate insulating film covering said first gate insulating film in said regions not covered with said gate electrode, but does not specifically disclose an insulating film with a smaller film thickness in a region not covered with a gate electrode than one covered with a gate electrode.

Tanabe discloses (see fig. 3, par. 0077 and claim 1) a silicon nitride insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode.

Since Yamazaki and Tanabe are both from the same field of endeavor, Thin Film Transistors, Tanabe's teachings would have been recognized in Yamazaki's pertinent art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yamazaki's device by incorporating Tanabe's teachings, since that would enlarge dielectric constant minimizing leakage as taught by Tanabe.

Regarding claim 17, Tanabe discloses a second insulating film having a smaller film thickness from an end position of said gate electrode covering said second insulating film.

6. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa in view of Tanabe.

Ogawa discloses figs. 1-6 a thin film transistor comprising semiconductor film or poly-

silicon film (as in claim 15), a first gate insulating film 3 or silicon oxide film (as in claim 14), a second gate insulating film 4 and a gate electrode 5 sequentially formed on one major surface of a substrate in that order, and an interlayer insulating film having a thickness larger than that of said second gate insulating film in a region covered with said gate electrode, said interlayer insulating film covering said gate electrode and covering said second gate insulating film in a region where said gate electrode is not formed, and wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is made of a material or silicon nitride film (as in claim 14) for supplying hydrogen to said semiconductor film, and said second gate insulating film covering said first gate insulating film in said regions not covered with said gate electrode, but does not specifically disclose an insulating film with a smaller film thickness in a region not covered with a gate electrode than one covered with a gate electrode.

Tanabe discloses (see fig. 3, par. 0077 and claim 1) a silicon nitride insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode.

Since Ogawa and Tanabe are both from the same field of endeavor, Thin Film Transistors, Tanabe's teachings would have been recognized in Ogawa's pertinent art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Tanabe's teachings with Ogawa's device, since that would enlarge dielectric constant minimizing leakage as taught by Tanabe.

As for the said second gate insulating film being integrally formed over said first gate insulating film recited in claim 13, it carries no patentable weight In re Larson 144 USPQ 347 (CCPA 1965) (the term "integral" did not define over a multi-piece structure secured as a single

unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.)

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
November 18, 2005

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800